What is claimed is:

Sub a1

1. A method comprising:

implementing an integrated circuit device within an electronic system, the integrated circuit device including an override disable pin; and

preventing modification of a representation of a primary pass-phrase when the override disable pin is asserted, the primary pass-phrase permitting access to stored information within the electronic system.

2. The method of claim 1, wherein the integrated circuit device comprises a package to form a packaged integrated circuit device.

3. The method of claim 1, wherein preventing of the modification of the primary pass-phrase includes

setting a control storage element within the integrated circuit device upon assertion of the override disable pin; and

disabling modification of the primary pass-phrase when the control storage element is set.

4. The method of claim 3, wherein the control storage element is set after placing the electronic system in an administration mode upon correctly inputting the primary pass-phase into the electronic system.

5. The method of claim 1, wherein the integrated circuit device further includes an override pin which, when asserted, allows a stored representation of the primary pass-phrase to be modified.

6. The method of claim 1, wherein the preventing of the modification of the primary pass-phrase includes signaling a control application software initiating a request for modification of the pass-phrase that a user is denied access to the stored information of the integrated circuit device unless the primary pass-phrase is correctly entered.

7. The method of claim 1, wherein the representation of the primary pass-phrase includes a hash value of the primary pass-phrase.

8. The method of claim 1, wherein control storage element includes at least one control register configured for permanent state retention over a plurality of power cycles.

9. A method comprising:

enabling access to stored information within an electronic system upon assertion of an override disable pin of an integrated circuit device; and

disabling access to the stored information despite assertion of the override pin of the integrated circuit device when an override disable pin of the integrated circuit device is asserted prior to assertion of the override pin.

10. The method of claim 9, wherein the integrated circuit device comprises a package to form a packaged integrated circuit device.

11. The method of claim 9, wherein the act of disabling access comprises

setting a control storage element within the integrated circuit device in response to the assertion of the override disable pin; and

determining whether the control storage element is set.

12. The method of claim 11, wherein the control storage element is set after placing the electronic system in an administration mode upon correctly inputting the primary pass-phase into the electronic system.

13. The method of claim 9, wherein the setting of the control storage element includes setting a bit of at least one control register configured for permanent state retention over a plurality of power cycles.

14. A method comprising:

enabling placement of an electronic system into an administrator mode upon assertion of an override disable pin of an integrated circuit device; and

disabling placement of the electronic system into the administrator mode despite assertion of the override pin of the integrated circuit device when an override disable pin of the integrated circuit device is asserted prior to assertion of the override pin.

15. The method of claim 14, wherein the integrated circuit device comprises a package to form a packaged integrated circuit device.

16. The method of claim 14, wherein the act of disabling access comprises

setting a control storage element within the integrated circuit device in response to the assertion of the override disable pin; and

determining whether the control storage element is set.

17. The method of claim 14, wherein the setting of the control storage element includes setting a bit of at least one control register configured for permanent state retention over a plurality of power cycles.

18. An electronic system comprising:

a bus;

a processor coupled to the bus;

a system memory coupled to the bus; and

an integrated circuit device coupled to the bus, the integrated circuit device including:

a memory,

an override pin to enable access to information stored within the memory upon assertion of the override pin, and

an override disable pin to disable access to the information stored within the memory despite the assertion of the override pin when the override disable pin is asserted prior to assertion of the override pin.

19. The electronic system of claim 18, wherein the integrated circuit further comprises a package to contain the memory from which the override pin and the override disable pin protrude.

20. The electronic system of claim 18, wherein the memory of the integrated circuit device is non-volatile memory.

21. The electronic system of claim 18, wherein the integrated circuit device further includes a control storage element.

22. The electronic system of claim 21, wherein the control storage element of the integrated circuit device includes at least one control register configured for permanent state retention over a plurality of power cycles.

23. The electronic system of claim 18, wherein the integrated circuit device further includes a microcode to determine whether the override disable pin has been asserted prior to assertion of the override pin.